(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 544 915 A1**

(12) **EUROPEAN PATENT APPLICATION published in accordance with Art. 158(3) EPC**

(21) Application number: **92911102.9**

(51) Int. Cl.5: **H01L 23/12**

(22) Date of filing: **11.06.92**

(86) International application number:
PCT/JP92/00745

(87) International publication number:
WO 93/00705 (07.01.93 93/02)

(30) Priority: **20.06.91 JP 176184/91**
08.05.92 JP 143558/92

(43) Date of publication of application:
09.06.93 Bulletin 93/23

(84) Designated Contracting States:
DE FR GB

(71) Applicant: **IWAKI ELECTRONICS CO., LTD.**
36-11, Shinbashi 5-chome, Minato-ku
Tokyo 105(JP)
Applicant: **FUJI ELECTROCHEMICAL CO.LTD.**
36-11 Shinbashi 5-chome
Minatoku Tokyo 105(JP)

(72) Inventor: **YAMAMOTO, Hiroyasu**
141-30, Kamanomae, Nagaya-machi, Mamiyu, Jyoban
Iwaki-shi, Fukushima 972(JP)
Inventor: **KONUMA, Takayuki**
67-48, Keisei, Yumoto-machi, Jyoban
Iwaki-shi, Fukushima 972(JP)
Inventor: **SHIKA, Akira**
36, Hachimancho, Toyoma, Taira
Iwaki-shi, Fukushima 970-02(JP)
Inventor: **SUZUKI, Hiroyoshi**
13, Nishi-machi, Katouno, Touno-machi
Iwaki-shi, Fukushima 979-01(JP)
Inventor: **KATOUNO, Masanori**
22-5, Nishidonocho, Kubota, Nakoso-machi
Iwaki-shi, Fukushima 979-01(JP)
Inventor: **SATO, Kaori**
80-191, Aza-Waseda, Kurosuno, Izumi-machi
Iwaki-shi, Fukushima 970-04(JP)

(74) Representative: **Charlton, Peter John**
Elkington and Fife Prospect House 8
Pembroke Road
Sevenoaks, Kent TN13 1XR (GB)

(54) **PACKAGE STRUCTURE OF SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR.**

(57) A package structure in which a conductive layer is provided on the under side of a circuit board, a semiconductor device are mounted on the top side, and both airtightness and electromagnetic shielding capability are satisfied by the connection with conductive sealing parts through conductive through holes. With respect to the electrode structure for external connection, protruding parts of high temperature solder are formed for the adaption to the surface mounting.

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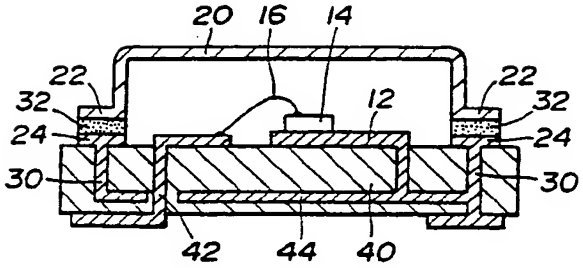
FIG. 3



BACKGROUND OF THE INVENTION

The present invention relates to package structure used to air-tightly seal a semiconductor device by covering the same with a conductive cap, and a method of manufacturing such package structures, and more particularly to a multi-electrode leadless package structure, such as hybrid IC, and an externally connecting electrode structure for an electronic part in a leadless package structure.

According to the present invention, a conductive layer is provided on the lower side of a circuit substrate on the upper surface of which a semiconductor element is mounted, and it is connected to a conductive seal member via conductive through-holes, whereby a seal structure having both air-tightness and electromagnetic shielding characteristics is provided, and the present invention also provides an externally connecting electrode structure used for an electronic part in a leadless package structure and capable of carrying out a surface mounting operation smoothly by utilizing projections made of high-temperature solder.

In a semiconductor device (for example, a hybrid IC) in which various types of semiconductors are mounted, air-tight sealing is carried out for the purpose of shutting off the semiconductors from the outside air. In a semiconductor device in which oscillating modules are mounted on the same circuit substrate, the provision of electromagnetic shielding characteristics are also required in addition to the air-tight sealing characteristics.

A metal case sealed by a resistance welding method (Japanese Utility Model Laid-open No. 2-33482/1990) is generally known as a package structure having both the air-tight sealing characteristics and electromagnetic shielding characteristics as mentioned above.

This metal case has a combination of an external lead-retaining stem and a cap. In this metal case, a semiconductor device formed by setting a semiconductor element on a circuit substrate and bonding the former to the latter with a gold wire is fixed to a stem, and a cap is put on the resultant product so as to seal the same.

A package structure produced by forming a second conductive layer on an intermediate layer provided on a circuit substrate, putting a flangeless cap on the resultant product, and soldering the end surface of the outer circumferential portion of the circuit substrate to electrically connect the second conductive layer and cap together and electromagnetically shield the product is disclosed in Japanese Utility Model-open No. 2-13796/1990.

In the former package structure out of these prior art package structures, a metal case (stem and cap) in which the circuit substrate is housed is required, and this necessarily causes the manufacturing cost and the weight of the product to increase. Moreover, a dedicated sealing apparatus is indispensable for the production of this package structure. Therefore, it is very difficult for this package structure to meet a demand, which has been made in recent years, to reduce the weight, height, length and width thereof.

The latter package structure is formed by merely putting a cap on the circuit substrate, so that the dimensions and weight thereof can be reduced. However, since the cap is soldered to the end surface of the circuit substrate, it is necessary to separate the circuit substrate into parts and seal the parts seperately, so that the operation efficiency becomes low. Therefore, this package structure is not suitable for the mass production of the devices of this kind.

In an electronic part having a plurality of semiconductor elements mounted on a single substrate, and a plurality of external electrodes, such as a hybrid IC, it is important to miniaturize a package and reduce the packaging area to improve the packaging density. Although various package structures have been developed, a leadless package structure is basically most advantageous in order to reduce the packaging area as shown, for example, in Japanese Patent Laid-open No. 53-84681/1978.

Various structures of an external electrode in a conventional leadless package have also been developed. These structures include, for example, a structure (Japanese Utility Model Laid-open No. 58-168141/1983) in which the circuit pattern provided on the connecting surface (bottom surface) of a ceramic substrate is used as an external electrode, as well as a structure (Japanese Uitlity Model Laid-open No. 2-114941/1990) in which projections of regular solder are formed on a conductive pattern provided on the connecting surface of a ceramic substrate and used for forming an external electrode thereon. Such leadless parts are mounted on a mother board (printed circuit board: PCB) and soldered to a circuit pattern by a reflow method or by a flow method, whereby the electrical and mechanical connection of the parts is carried out.

In these external electrode structures, the ceramic substrate and mother board (PCB) are liable to closely contact each other during a mounting operation, so that it is impossible to visually ascertain the electrical connection of leadless part to circuit pattern via solder. Even when the package structure is washed, flux remains thereon or solder balls (excess solder in the form of balls) are deposited thereon, and

this would cause short-circuiting to occur. Moreover, since the ceramic substrate and mother board (PCB) have different thermal expansion coefficients and Young's moduli, flexure occurs easily in the connected portions of these substrates due to the stress occurring therein and attributable to the heat cycle, and due to the deformation thereof, such as a warp thereof.

A structure which is capable of partially solving these problems, and which uses hemispherical projections of conductive rubber as external electrodes, has also been proposed as disclosed in Japanese Patent Laid-open No. 59-96751/1984. In this external electrode structure, the flexure of the ceramic substrate and mother board can be prevented by the conductive rubber but solder cannot be used to connect a leadless part to the mother board. Therefore, a leadless part is necessarily pressed against the mother board by an auxiliary means or a thermocompression bonding method is necessarily employed. Moreover, it is necessary that the projections of conductive rubber be fixed one by one to predetermined portions of a ceramic substrate, with the result of extended man-day.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a package structure for semiconductor devices, capable of eliminating the above-described drawbacks of the prior art structures, having both excellent air-tightness and excellent electromagnetic shielding characteristics, capable of being formed to smaller dimensions and weight, and capable of being mass-produced at a low cost owing to the simple construction and a high sealing efficiency thereof.

Another object of the present invention is to provide an external electrode structure for leadless packages, capable of carrying out the electrical and machanical connection of parts with a high reliability, capable of visually ascertaining the connection of parts, free from the problems of the occurrence of residue of flux and solder balls, and having a high productivity owing to the possibility of employing a single-step manufacturing method.

The present invention is basically directed to a package structure for semiconductor devices, which is used to cover a semiconductor device, in which a semiconductor element is mounted on the upper surface of a circuit substrate, with a conductive cap so as to air-tightly seal the semiconductor device. In such a package structure, the cap is formed so as to have a flange at the circumferential portion thereof, and the circuit substrate has a first conductive layer on the portion of the upper surface thereof which corresponds to the flange of the cap, a second conductive layer covering the lower surface thereof, and a plurality of conductive through-holes distributed at substantially regular intervals just under the first conductive layer and connecting the first and second conductive layers together. The joint portions of the flange and first conductive layer are sealed with a conductive sealing material.

The first conductive layer is usually formed so that it is in the shape of a frame extending along the outer circumference of a circuit substrate. In the case where a single-layer circuit substrate is used, a second conductive layer is formed on the substantially whole portion of the lower surface thereof except the portion of the same surface on which the lead electrodes of a semiconductor device are provided. The package structure according to the present invention is used specially suitably for, for example, a hybrid IC.

An air-tightly sealed structure is attained by sealing the flange of a cap and the first conductive layer on a circuit substrate with a conductive sealing material. Since a sealing operation is carried out on the upper surface of a circuit substrate, a plurality of package structures can be obtained at a time. The electromagnetic shielding of the package structure is done with a cap at the upper portion thereof, and with a conductive sealing material, a first conductive layer, conductive through-holes and a second conductive layer at the side and lower portions thereof. The conductive through-holes serving as the electromagnetic shielding members at the side portions of a package structure are positioned just under the first conductive layer. Accordingly, the area of the circuit substrate does not increase to a level higher than a required level, and this contributes to the saving of space.

The present invention is also directed to an external electrode structure for leadless packages, which has projections consisting of high-temperature solder of a melting point of 240° - 330°C and formed on an external electrode-forming conductive pattern provided on the connecting surface of a ceramic substrate used in a leadless package. It is recommended that the projections consisting of high-temperature solder be formed to a hemispheric shape or to a shape similar thereto, and to a height of around 0.2 - 1.0 mm. More preferably, each projection is formed to a frusto-hemispherical shape having a flat free end portion. When the projections are formed in this manner, an excellent self-aligning effect can be expected during a reflow soldering operation. The external electrode-forming conductive pattern is formed, for example, to a polygonal shape having not less that four apexes, a polygonal shape having an arcuate side, and a circular shape. The conductive pattern of such shapes may be produced by shaping a conductive material alone, or

by shaping the openings in an organic or inorganic insulating layer formed on a conductive material. An external electrode-forming conductive pattern may be formed by providing a metallized layer of Mo-Mn (molybdenum - manganese) or W (tungsten) or a metallized layer of Cu (copper), Ag-Pd (silver - palladium), Pt-Ag (platinum - silver), and then forming thereon projections of high-temperature solder.

In order to produce such external electrodes, a non-separated ceramic substrate from which a plurality of leadless parts are to be formed is prepared, and external electrode-forming conductive patterns are then formed on one surface of this substrate, projections which consist of high-temperature solder being formed at once on the conductive patterns by a reflow method or a flow method. The substrate is thereafter divided to obtain leadless parts. In order to connect a leadless part thus obtained to a packaging substrate, the former is mounted on the latter, and the projections consisting of high-temperature solder and the wiring pattern on the mother board may be connected together by using regular solder, i.e., by melting regular solder alone by heating the same to a temperature at, or higher than the melting point of the regular solder and lower than the melting point of the high-temperature solder.

In the preferrd embodiments of the present invention, the external electrodes have projections of high-temperature solder. Therefore, the projections are not melted in the leadless part-connecting step using regular solder, so that a clearance corresponding to the height of each projection occurs between the ceramic substrate and mother board. This enables the ascertainment of the connection of the leadless part to be carried out visually after the mounting operation has been completed, and the problems of deposition of flux residue and solder balls which are liable to occur during a washing operation to be eliminated. The projections of solder and the clearance mentioned above serve to lessen the flexure of the connected portion of the part which is liable to occur due to the temperature cycle and a warp of the substrates.

Furthermore, the external electrode structure using solder enables a plurality of projections to be formed at once, and the electrical and mechanical connection of a leadless part by means of regular solder during a mounting operation to be effected reliably.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view of a package structure according to an embodiment of the present invention;
Fig. 2 is a plan view of a circuit substrate used in the package of Fig. 1;
Fig. 3 illustrates another embodiment of the package structure;
Figs. 4A and 4B are a front elevation and a bottom view, respectively, of a first embodiment of the external electrode structure according to the present invention;
Figs. 5A and 5B are a front elevation and a bottom view, respectively, of another embodiment of the external electrode structure;
Figs. 6A and 6B are a front elevation and a partially cut-away bottom view, respectively, of still another embodiment of the external electrode structure;
Fig. 7 is a pratially cut-away bottom view of a further embodiment of the external electrode structure;
Fig. 8 illustrates another embodiment of the external electrode structure;
Fig. 9 is a perspective view showing the shape of still another embodiment of the external electrode structure;
Figs. 10 and 11 illustrate the methods of forming external electrode structures; and
Fig. 12 illustrates a method according to the present invention of fixing a leadless part to a mother board.

PREFERRED EMBODIMENTS OF THE INVENTION

Fig. 1 is a sectional view showing an embodiment of the package structure for semiconductor devices according to the present invention, and Fig. 2 a plan view of a circuit substrate in this package structure. This embodiment uses a single-layer circuit substrate. A circuit substrate 10 consists of a alumina or aluminum nitride. A circuit pattern 12 is provided on the upper surface of the circuit substrate 10, and a semiconductor element 14 of one of various types is mounted thereon, the circuit pattern 12 and semiconductor element 14 being then connected together with a gold wire 16 to form a semiconductor device. A region (designated by a reference numeral 18) shown by one-dot chain lines in Fig. 2 is a portion on which the semiconductor device is formed. A metal cap 20 is put on the resultant circuit substrate 10. In this embodiment, the cap 20 has a flange 22 projecting from a lower end portion of the outer circumference thereof in the horizontally outward direction, and this cap is plated entirely with nickel.

In this embodiment, a frame-shaped first conductive layer 24 is formed on the portion of the upper surface (semiconductor element-mounting surface) of the circuit substrate 10 which corresponds to the flange 22, and a second conductive layer 28 on the lower surface of the substrate 10 so as to cover the

substantially whole thereof, except a portion on which a lead electrode 26 is formed and a portion which is close to this electrode 26. A plurality of conductive through-holes 30 are formed just under the first conductive layer 24 to connect the first and second conductive layers 24, 28 together. These conductive through-holes 30 are distributed substantially uniformly in the circumferential portion of the circuit substrate 10. Twelve through-holes 30 are formed at substantially regular intervals in this embodiment. These conductive layers can be formed easily by thick film printing, etching, selective plating, laminating, and through-hole techniques.

In the practical operaional procedure, various types of conductive layers are formed first on the circuit substrate 10 as mentioned above, and the semiconductor element 14 is then mounted thereon to produce a semiconductor device. A conductive sealing material 32 of, for example, a tin - lead solder preform is then placed on the first conductive layer 24, and then flange 22 of the cap 20 thereon via this sealing material 32. Thus, a package structure having both satisfactory air-tightness and satisfactory electromagnetic shielding characteristics can be obtained.

It is also possible to print the first conductive layer with tin - lead solder paste as a conductive sealing material 32 and form a solder layer through a reflow furnace. When, for example, high-temperature solder having a high heat resistance or conductive filler-containing sealing glass is used as a conductive sealing material with tin - lead regular solder applied to the lower surface of the circuit substrate to form a lead electrode, a package structure compatible with SMD (surface-mounted device) as well is produced.

According to the present invention, a cap is combined with a circuit substrate at the upper surface of the latter. Therefore, the invention can employ the steps of forming, in a series-arranged state at once on a single substrate, a plurality of circuit substrate parts having the above-mentioned conductive layers and conductive through- holes, and mounting semiconductor elements on the respective circuit substrate parts to form semiconductor devices, fixing metal caps sequentially to the resultant semiconductor devices, and then cutting the substrate so that the semiconductor devices are separated from one another. This enables semiconductor devices to be manufactured in large quantities at a low cost.

Fig. 3 is a sectional view of another embodiment of the present invention. This embodiment uses a multilayer circuit substrate. Since the basic construction of this embodiment is identical with that of the previously-described embodiment, the corresponding parts are designated by the same reference numerals, and detailed descriptions of such parts are omitted. A circuit substrate 40 is provided with a circuit pattern 12 on the upper surface thereof, and a frame-shaped first conductive layer 24 is formed on the portion of the substrate which corresponds to a flange 22. In this embodiment, a second conductive layer 44 is formed so as to constitute, substantially entirely, an intermediate layer, except the portions which correspond to conductive through-holes 42 for the leads and the portions which are close to these holes 42. A plurality of conductive through-holes 30 are formed just under the first conductive layer 24 to connect the first conductive layer 24 and the second conductive layer 44, which constitutes an intermediate layer, together. These conductive through-holes 30 are distributed substantially uniformly in the circumferential portion of the circuit substrate 40. A semiconductor element 14 is mounted on the circuit substrate 40, and connected thereto with a gold wire 16 to form a semiconductor device. The flange 22 of a cap 20 is then placed on the first conductive layer 24 via a conductive sealing material 32, whereby the cap is combined with the semiconductor device.

The present invention can also be applied to the case where a cap is put on a semiconductor device, which is formed in part of a large circuit substrate, to air-tightly seal and electromagnetically shield the semiconductor device.

According to the present invention, a cap having a flange at the circumferential portion thereof is used as described above, and a first conductive layer is formed on the portion of the upper surface of a circuit substrate which corresponds to the flange, the flange and first conductive layer being sealed with a conductive sealing material. Therefore, the semiconductor device can be air-tightly sealed. The circuit substrate has a second conductive layer covering the lower surface thereof, and a plurality of uniformly distribute conductive through-holes connecting these two conductrive layers together, and uses a conductive cap and a conductive sealing material. Accordingly, the upper portion of the package structure is enclosed with the cap, and the side and lower portions thereof are enclosed with the conductive sealing material, first conductive layer, conductive through-holes and second conductive layer. Thus, the package structure is electromagnetically shielded.

Since the conductive through-holes connecting the first and second conductive layers together in the present invention are positioned just under the first conductive layer, the size of the circuit substrate can be reduced to the lowest possible level required for the air-tight sealing of a package structure, so that the space can be saved. Since a metal stem having large weight is unnecessary, the weight of a package structure can be reduced. Moreover, a package structure easily compatible with SMD (surface-mounted

device) is permitted by the construction of the circuit substrate.

According to the present invention, a cap is sealed to the upper surface of a circuit substrate. Therefore, the present invention can have the steps of forming a plurality of circuit substrate parts in a series-arranged state at once on a single substrate, forming semiconductor devices on these substrate parts, placing caps sequentially on these semiconductor devices and sealing the same, and finally cutting off the packaged structures from one another. Accordingly, the present invention is suitable for the mass production of package structures and enables the cost of manufacturing the same to be reduced.

The embodiments of the external electrode structure for leadless packages according to the present invention will now be described.

Referring to Figs. 4A and 4B, which show an embodiment of the external electrode structure for leadless packages according to the present invention, a plurality of semiconductor elements (not shown) are mounted on a ceramic substrate 50, and a cap 20 is placed on the resultant substrate and sealed to form a hermetically sealed leadless part 54. External electrode-forming conductive patterns 52 are provided along two opposite sides of a connecting surface (lower surface) of the ceramic substrate 50, and hemispherical projections 56 of high-temperature solder having a melting point of 240° - 330°C are formed on these conductive patterns 52, these projections being used as external electrodes, that is, electrodes for connecting the leadless part 54 to a mother board (PCB).

In the embodiment of Figs. 4A and 4B, the circular conductive patterns 52 on which the projections 56 are provided are defined by a conductive material alone. The conductive patterns are formed circularly because such circular conductive patterns enable the projections to be swollen hemispherically, and the bonding strength and the height thereof are increased. The projections 56 are formed so that the height t thereof becomes around 0.2 - 1.0 mm. When a clearance substantially corresponding to this height remains between the ceramic substrate and mother board, the portions of a part connected with solder can be visually ascertained and the flux and solder balls can be removed easily. The high-temperature solder used in the present invention includes In-Pb solder containing 30% by weight of In (indium) or less, Pb solder containing 85% by weight of Pb (lead) or more, and Pb-Sb or Sn-Sb solder containing 15% by weight of Sb (antimony) or less. The conductive pattern may be formed to a polygonal shape having four apexes or more and a polygonal shape having some arcuate sides in addition to a circular shape referred to above.

The configuration of the external electrodes may be arbitrarily determined. When a certain number of external electrodes are to be provided, the projections 56 of high-temperature solder may be formed along four sides or circumferential portions of the packaging surface of a ceramic substrate 50 as shown in Figs. 5A and 5B. The projections may also be formed in a latticed arrangement, an illustration of which is omitted, on the connecting surface of the ceramic subtrate.

Figs. 6A, 6B and 7 show examples of the shapes, which are defined by those of the openings in the insulating layers 62 formed on a conductive material 60, of the conductive patterns on which the projections 56 of high-temperature solder are formed. In the example of Figs. 6A and 6B, the opening is formed circularly, and, in the example of Fig. 7, the opening is formed hexagonally. The insulating layer 62 may be formed by using an organic material, or an inorganic material, such as glass.

There is also an external electrode structure in which projections 56 of high-temperature solder are formed on metallized layers 64 of Mo-Mn (Molybdenum-manganese) or W (tungsten) provided as a conductive layer used for the formation of external electrodes, as shown in Fig. 8. These metallized layers 64 are formed by applying paste of the above-mentioned material to a circuit substrate by a screen printing method, and firing the paste at a high temperature of one thousand several hundred degrees centigrade. Providing such metallized layers 64 is preferable because these materials, which are also used for leads, have a very high bonding strength with respect to solder, and enable the height of the projections to be increased by the thickness of the metallized layers 64. In order to reduce the manufacturing cost, metallized layers of Cu, Ag-Pd or Pt-Ag, the firing temperature should be set to 850° - 900°C.

The projections constituting the external electrodes may be domed at the free end portions thereof, i.e., formed hemispherically as shown in Figs. 4A and 5A, and more preferably, they are formed frusto-hemispherically so that the projecting end portions thereof have flat surfaces 56a as shown in Fig. 9. The reason resides in the discovery by the inventors of the present invention that, when the projections are formed hemispherically, they pointcontact the mother board, so that a satisfactory self-aligning effect of the projections during a solder reflow operation is not obtained, whereby a high mounting accurancy of the electronic parts may not be obtained. On the other hand, when flat surfaces 56a are formed as shown in Fig. 9, an electronic part moves to proper position after a solder reflow operation has been completed even if the electronic part deviates from a proper position when it is mounted on a solder pad. Namely, when a solder reflow operation is carried out with the electronic part left deviating from the mounting position, the electrodes of Fig. 9 are drawn to the center of the pad owing to the surface tension of the solder being

melted, whereby the electronic part is mounted on the proper position.

Table 1 shows the results of measurement of the amounts of deviation, which occurs after a solder reflow operation has been completed, of ten examples of electronic parts with the level of deviation of these parts prior to the solder reflow operation set to 0.4 mm. The results in Table 1 show that, when projections formed to a flat surface-carrying hemispherical shape as shown in Fig. 9 are employed, the deviation occurring after a solder reflow operation has been completed of all the examples decreases to 0.3 mm or less to enable the electronic parts to be mounted with a very high accuracy. Out of the examples which employ projections formed to an ordinary hemispherical shape as shown in Fig. 12, four examples deviated 0.5 mm after the completion of a solder reflow operation.

Table 2, similar to Table 1, shows the results of measurement conducted with level of deviation of examples prior to a solder reflow operation set to 0.7 mm. All the examples in Table 2 that employ flat surface-carrying projections have a decreased level of deviation of 0.3 mm or less and can display a satisfactory self-aligning effect, while more than a half of the examples which employ hemispherical projections having no flat surfaces have a slightly increased level of deviation of the position for mounting a part.

As is clear from the above, it is desirable that the projections constituting external electrodes be formed so that each thereof has a flat surface-carrying hemispherical body shown in Fig. 9.

Table 1

(Relation, which is determined when the deviation of the part-mounted position prior to the solder reflow operation is set to 0.4 mm, between the shape of projections and a deviation of the part-mounted position occurring after the completion of the solder reflow operation)		
Deviation of part-mounted position after the completion of a solder reflow operation (mm)	Shape of projections	
	Frusto-hemispherical	Hemispherical
Not more than 0.05	One example	
0.1	Two Examples	
0.2	Two Examples	
0.3	Five Examples	One example
0.4		Five examples
0.5		Four examples

Table 2

(Relation, which is determined when the deviation of the part-mounted position prior to the solder reflow operation is set to 0.7 mm, between the shape of projections and a deviation of the part-mounted position occurring after the completion of the solder reflow operation)

Deviation of part-mounted position after the completion of a solder reflow operation (mm)	Shape of projections	
	Frusto-hemispherical	Hemispherical
0.1	One example	Three examples
0.2	Two Examples	Seven examples
0.3	Three Examples	
0.4		
0.7		
0.8		

A method of forming a plurality of projections will now be described. The formation of spherical projections shown in, for example, Fig. 4A will be described for the convenience of explanation. The projections 56 can be formed collectively at once by the methods shown in Figs. 10 and 11. In both of these methods, conductive patetrns 72 on which external electrodes are provided are formed on one surface of an undivided multi-substrate producing plate 70 (nine-substrate producing plate in this example) of a ceramic substrate 50, and projections 56 consisting of high-temperature solder are formed at one time on these conductive patterns 72. The example of Fig. 10 uses a reflow method, which has the steps of applying solder paste to the upper surfaces of the conductive patterns 72 on the ceramic substrate 50 by screen printing or by means of a dispenser, and passing the resultant product through a reflow apparatus so as to melt the high-temperature solder and swell the same to hemispherical shape by utilizing the surface tension therof. Since high-temperature solder is used, it is preferable to use a reflow apparatus capable of maintaining a nitrogen atmosphere.

Fig. 11 shows an example using a flow method, in which a ceramic substrate 50 having conductive patterns 72 thereon is passed through a flow apparatus (not shown) so as to deposit high-temperature molten solder on these patterns and swell the same to a hemispherical shape in the same manner as described above. In this method, a plurality of projections 56 of high-temperature solder which are to form external electrodes can be formed collectively at once on the multi-substrate producing plate 70, so that the productive efficiency is very high.

The connection of a leadless part having such projections 56 of high-temperature solder as external electrodes is carried out by the steps shown in Fig. 12. The connecting surface of a ceramic substrate 50 consituting a leadless part is directed to a mother board (PCB) 80, and the external electrodes (projections 56 of high-temperature solder) and wiring patterns 82 on the mother board 80 are opposed to and aligned with each other, regular solder (60 Sn/40Pb solder having a melting point of 183° - 188°C) being then heated to a temperature not lower than the melting point of the regular solder and lower than that of the high-temperature solder, whereby the leadless part is connected. In the example of Fig. 12, solder paste (regular solder) 84 is applied to the mother board 80, and the leadless part is connected by a reflow method. The connection of the part may also be carried out by a flow method. In any case, the regular solder 84 alone is melted, and the projections 56 consisting of high-temperature solder is left substantially as they are with the electrical and mechanical connection between the projections 56 and the wiring patterns 82 on the mother board 80 effected.

In the external electrode structure for leadless packages according to the present invention, the external electrodes are not melted while the leadless part is connected by using regular solder, so that a clearance corresponding to the height of the projections can be created between the ceramic substrate and mother board. This enables the visual ascertainment of the solder-connection of the leadless part to be carried out after the mounting of the part has been completed, and the washing of the electrode structure to be done without causing flux residue to occur and without causing the deposition of solder, which gives rise to short-circuiting, to occur. Even when stress is imparted to the connected portions of the part due to the flexure of the mother board or a difference between the thermal expansion coefficient of the ceramic substrate and that of the mother board, warping is reduced by the clearance between high-temperature solder projections and these substrates.

Moreover, since the external electrode structure is formed out of high-temperature solder, the projections constituting the external electrodes can be formed collectively at once. Therefore, the production of this electrode structure can be carried out easily with a high accuracy, and the productivity becomes high. Since regular solder can be used during the mounting of a leadless part, the electrical and mechanical connection of the projections with the wiring patterns can be obtained easily and reliably, and a highly reliable external electrode can be obtained.

Claims

1. In a package structure for semiconductor devices, in which a semiconductor device having a semiconductor element mounted on the upper surface of a circuit substrate is covered with a conductive cap and sealed air-tightly, an improvement characterized in that said cap has a flange at the circumferential portion thereof, said circuit substrate having a first conductive layer formed on the portion of the upper surface therof which corresponds to said flange, a second conductive layer covering the lower surface of said circuit substrate, and a plurality of conductive through-holes provided so as to be distributed substrantially uniformly just under said first conductive layer and connecting said first and second conductive layers together, the contact surfaces of said flange and said first conductive layer being

sealed with a conductive sealing material.

2. A package structure according to Claim 1, wherein said first conductive layer is formed in the shape of a frame so that said first conductive layer extends along the outer circumferential portion of said circuit substrate, said second conductive layer being formed on the substantially whole of the lower surface of said circuit substrate except the portion thereof which correspond to a lead electrode of said semiconductor device.

3. A package structure according to claim 1, wherein said first conductive layer is formed in the shape of a frame so that said first conductive layer extends along the outer circumferential portion of said circuit substrate, said second conductive layer being formed so as to constitute the substantially whole of an intermediate layer.

4. A package structure according to Claim 1, wherein conductive patterns on which external electrodes are to be formed are provided on the connecting surface of a ceramic substrate constituting said circuit substrate, and projections of high-temperature solder of a melting point of 240° - 330°C are formed on said conductive patterns.

5. An external electrode structure for leadless packages using a ceramic substrate, characterized in that projections consistig of high-temperature solder having a melting point of 240° - 330°C are formed on conductive patterns provided on a connecting surface of said ceramic substrate and used to form external electrodes thereon.

6. An external electrode structure accoridng to Claim 5, wherein the height of said projections of high-temperature solder is set to 0.2 - 1.0 mm.

7. An external electrode structure according to Claim 5, wherein said conductive patterns on which said external electrodes are to be formed are formed to a polygonal shape having not less than four apexes.

8. An external electrode structure according to Claim 5, wherein said conductive patterns on which said external electrodes are to be formed are formed to a polygonal shape having not less than four apexes and some arcuate sides.

9. An external electrode structure according to Claim 5, wherein said conductive patterns on which said external electrodes are to be formed have a circular shape.

10. An external electrode structure according to Claim 5, wherein said conductive patterns on which said external electrodes are to be formed are defined by a conductive material alone.

11. An external electrode structure according to claim 5, wherein said conductive patterns on which said external electrodes are to be formed are defined by the openings of an organic or inorganic insulating layer formed on a conductive material.

12. An external electrode structure according to Claim 5, wherein each of said projections of high-temperature solder is formed frusto-hemispherically so that said projection has a flat surface at the free end portion thereof.

13. An external electrode structure according to Claim 5, wherein metallized layers of molybdenum-manganese or tungsten, or metallized layers of copper, silver-palladium or platinum-silver are provided as conductive patterns on which said external electrodes are to be formed, said projections of high-temperature solder being formed on said metallized layers.

14. A method of manufacturing external electrodes for leadless packages, comprising the steps of forming conductive patterns, on which external electrodes are to be formed, on one surface of an undivided multi-ceramic-substrate producing plate, and forming projections of high-temperature solder on said conductive patterns at once.

15. A leadless part connecting method comprising the steps of mounting a leadless part having an external electrode structure defined in Claim 5 on a mother board, heating regular solder to a temperature not lower than a melting point thereof and lower than that of high- temperature solder so as to melt said regular solder alone, and connecting projections of high-temperature solder and wiring patterns on said mother board together.

FIG. 1

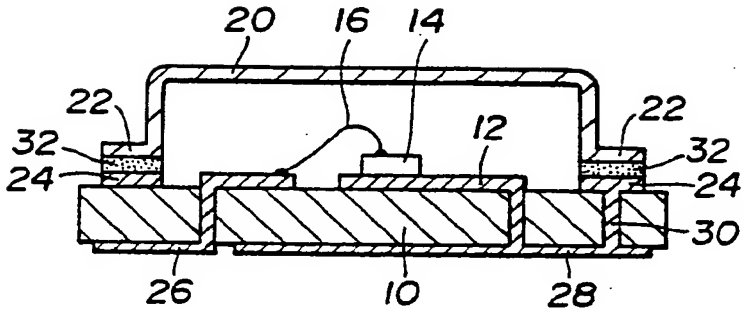


FIG. 2

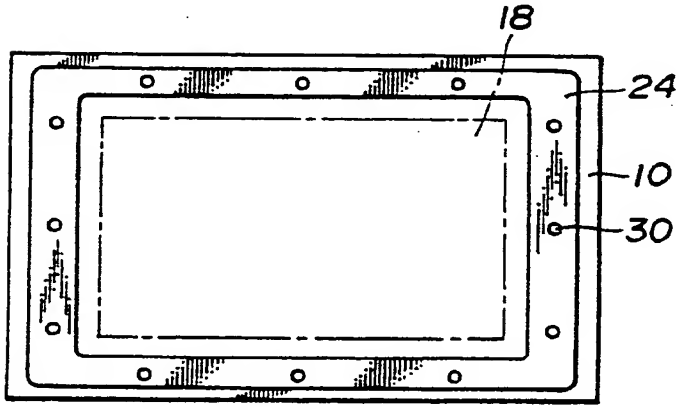


FIG. 3

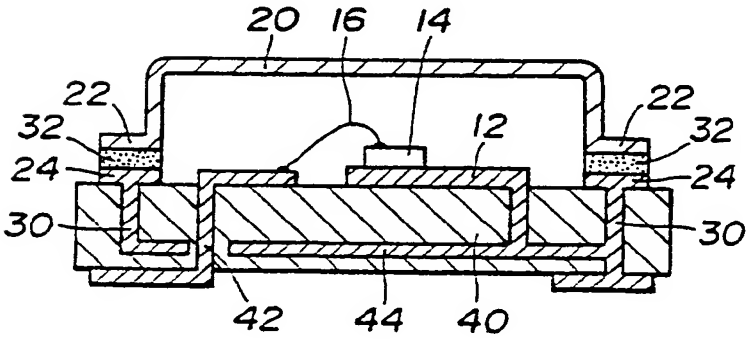


FIG. 4A

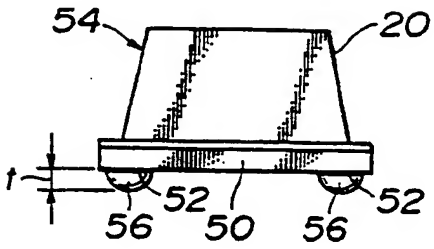


FIG. 4B

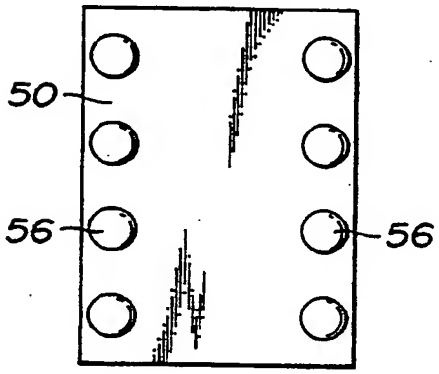


FIG. 5A

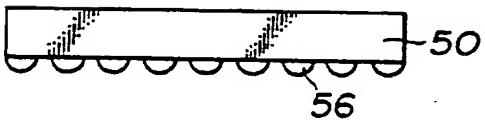


FIG. 5B

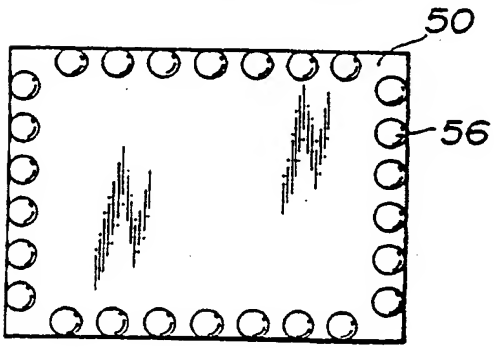


FIG. 6A

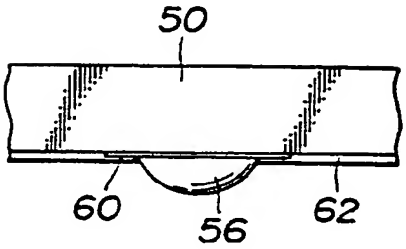


FIG. 6B

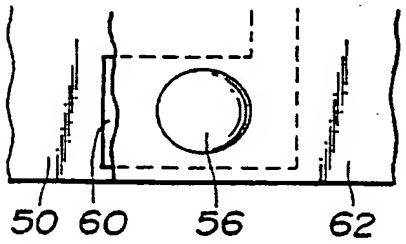


FIG. 7

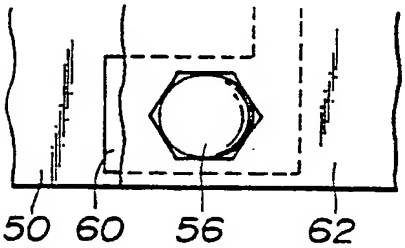


FIG. 8

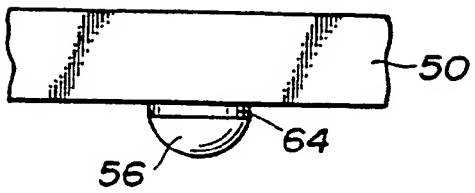


FIG. 9

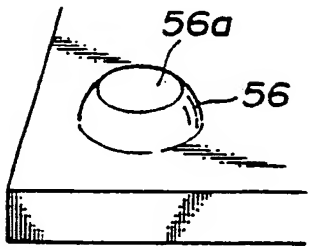


FIG. 10

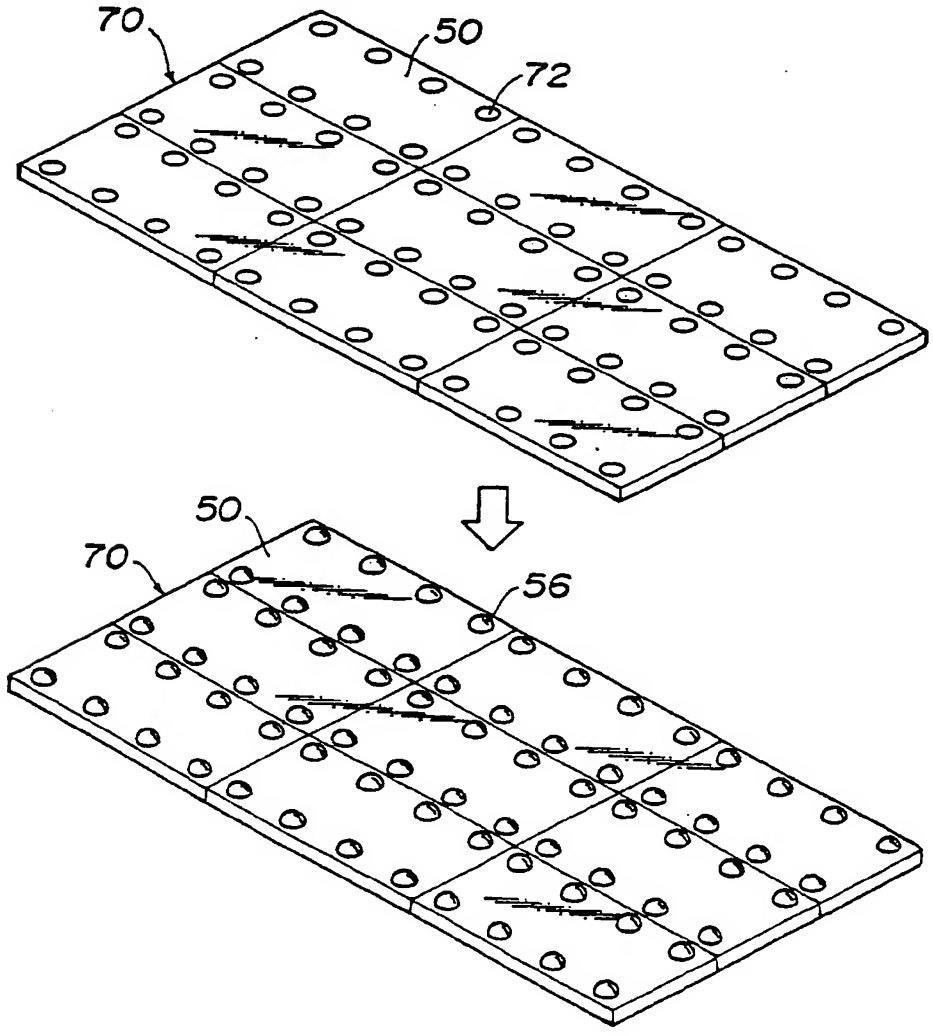


FIG. 11

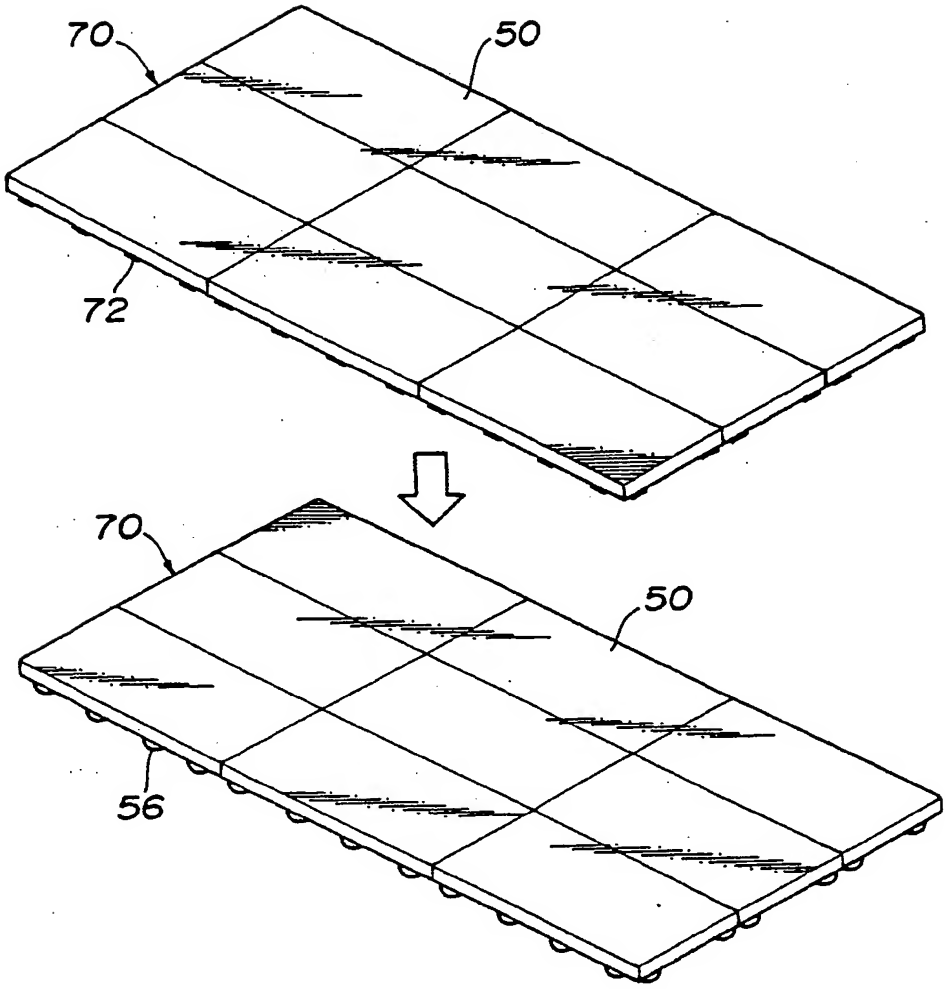
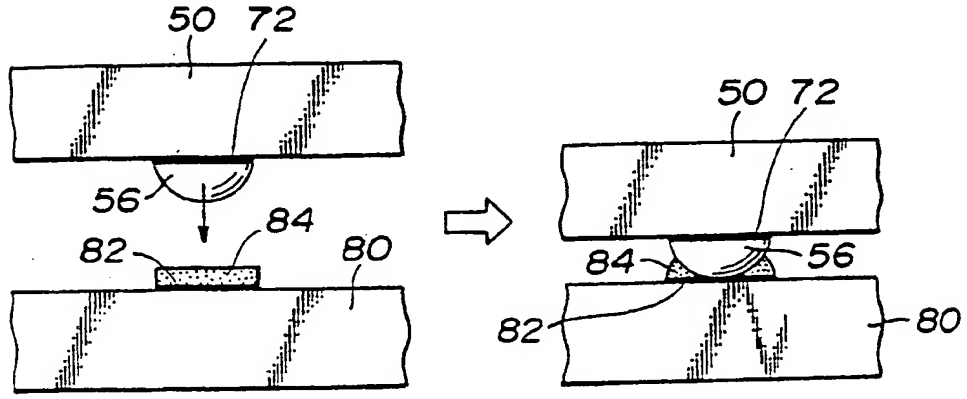


FIG. 12



INTERNATIONAL SEARCH REPORT

International Application No PCT/JP92/00745

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl[5] H01L23/12

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC	H01L23/60, H01L23/10

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

Jitsuyo Shinan Koho	1970 - 1992
Kokai Jitsuyo Shinan Koho	1971 - 1992

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	JP, A, 2-17659 (Digital Equipment Corp.), January 22, 1990 (22. 01. 90), & US, A, 3,303,392 & EP, A, 103,068 & DE, A, 2,749,848	1-5

* Special categories of cited documents: [10]

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
July 20, 1992 (20. 07. 92)	August 18, 1992 (18. 08. 92)
International Searching Authority	**Signature of Authorized Officer**
Japanese Patent Office	